

Fig - 1

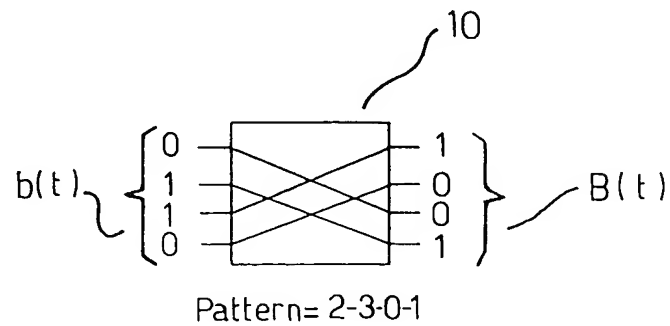


Fig - 2

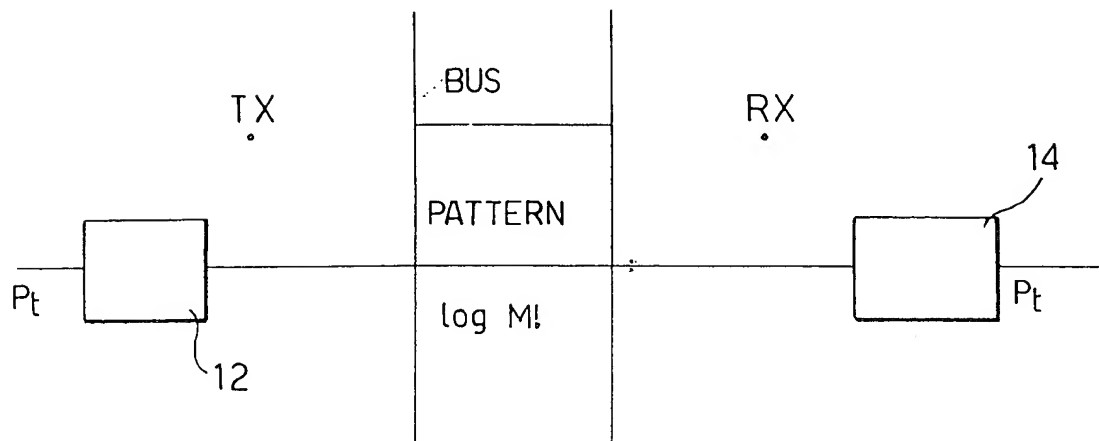
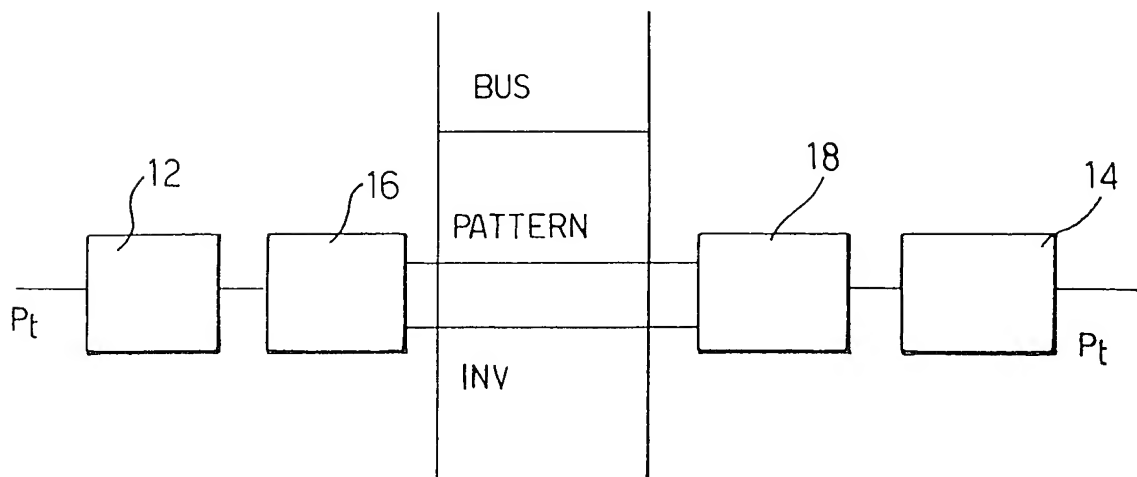


Fig - 3



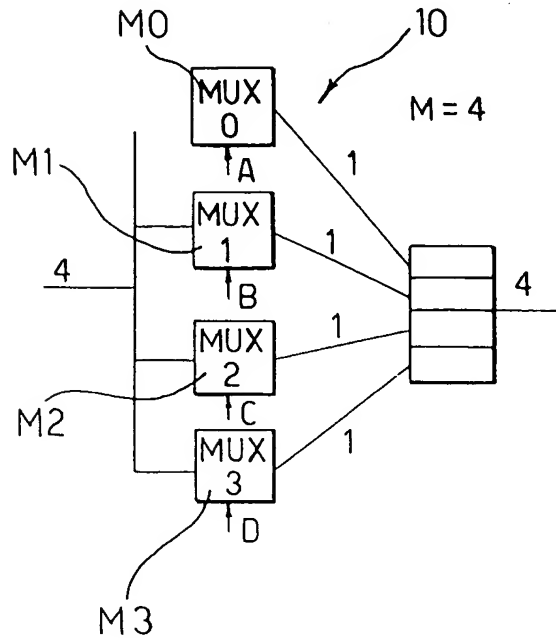


Fig. 4

Fig. 5

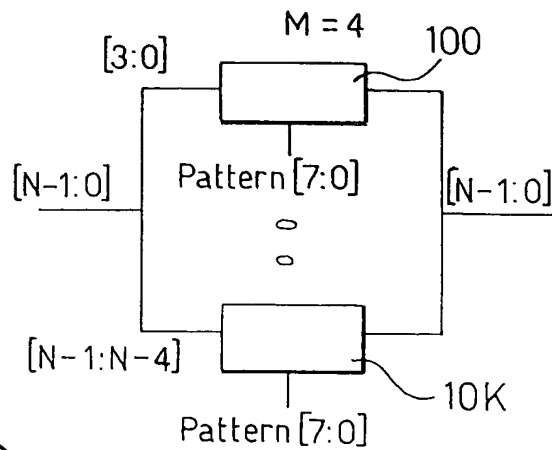
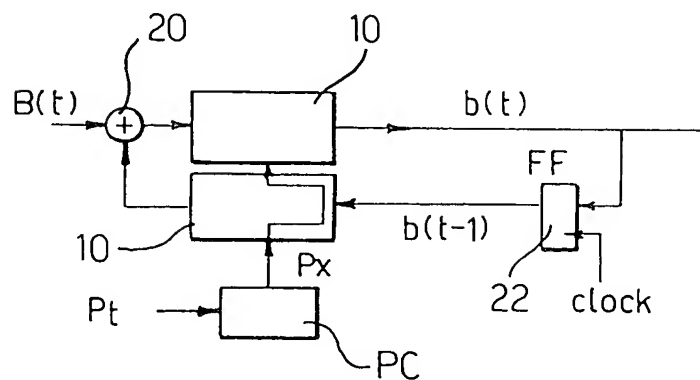
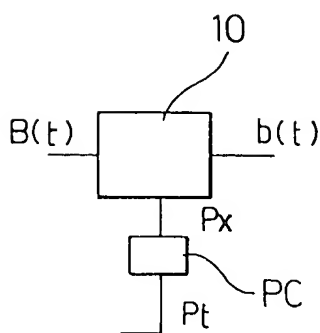


Fig. 6

Fig. 7



50

90

out_reg

clockxQ

$B(t-1)$

20

60

(*) Threshold Unit

70

PG

clockxQ

patt_reg

clockxQ

90

90

enable

80

score_reg

90

Figure 1 is a block diagram of a neural network architecture. The network consists of a sequence of blocks labeled 1000, 1001, 1002, ..., 100(L-1). Each block receives a "clock x Q" signal. Block 1000 outputs "out0", "out1", "out2", and "out(L-1)". Block 1001 outputs "B(t)". Block 1002 outputs "Scores 0..L-1". Block 100(L-1) outputs "b(t)" and "B(t-1)". A feedback loop connects "out(L-1)" back to "out0".

Fig. 12

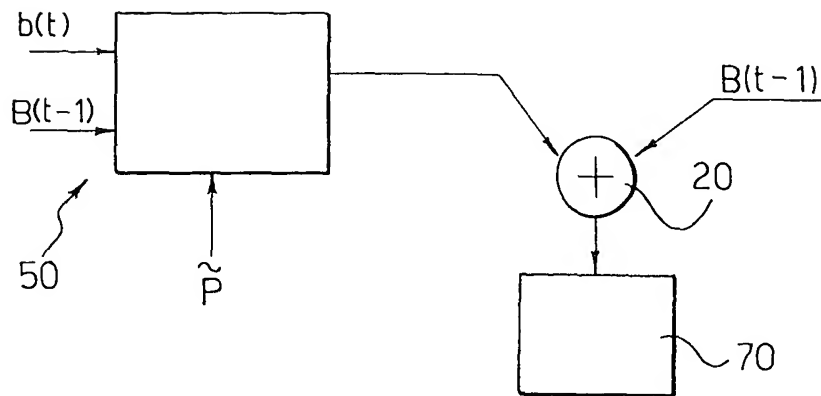


Fig. 13

